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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,871	05/17/2006	Kazuki Noda	59127US007	8302

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EXAMINER
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FORD, KENISHA V

ART UNIT	PAPER NUMBER
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2812

NOTIFICATION DATE	DELIVERY MODE
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02/26/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/595,871	<b>Applicant(s)</b> NODA ET AL.	
	<b>Examiner</b> KENISHA V. FORD	<b>Art Unit</b> 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 November 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/19/07</u> .  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

This Office Action is in response to the amendment filed on 30 November 2007. Currently, claims 1-20 are pending.

### ***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on 9/11/07 & 12/19/07 was filed after the mailing date of the Non-Final Rejection on 9/10/07. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

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3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Lu et al. (US 7,226,812 B2).

Regarding claim 1, Wolk et al. discloses a method for manufacturing a semiconductor chip comprising:

- Applying a photothermal conversion layer, referred to as a light-to-heat conversion (LTHC) layer, that can convert light energy to heat energy (col. 2, lines 4-7). The LTHC disclosed comprises a light-absorbing agent (radiation absorber) that converts the radiation into heat to enable transfer of the transfer layer to the receptor (light-transmitting support) (col. 6, line 1-col 7, line 3).
- Preparing a semiconductor wafer by laminating the wafer, with a circuit face and photothermal conversion layer (or LTHC layer) facing each other, and irradiating light from the light-supporting side to cure the photocurable adhesive layer to have a non-circuit face on the outside (col. 9, lines 6-23; col. 10, lines 5-11 and 28-32).

Wolk et al. does not teach the decomposing of the LTHC layer, a method for grinding the non-circuit face of the wafer, dicing the ground semiconductor wafer, or optionally removing the adhesive layer from the semiconductor chips.

Lu et al. discloses these limitations in its method of manufacturing a semiconductor chip comprising:

- Irradiation radiation energy to decompose the photothermal conversion layer (col. 6, lines 44-50)
- Grinding the non-circuit face of the semiconductor wafer (col. 7, lines 18-20)
- Dicing the ground semiconductor wafer from the non-circuit face side to cut it into a plurality of semiconductor chips (col. 7, lines 31-32)

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- Optionally removing the adhesive layer (Fig. 9, col. 6, lines 8-10).

Regarding claim **2**, Lu et al. discloses a method wherein a die bonding tape is affixed to the semiconductor wafer before dicing the ground semiconductor wafer (col. 6, lines 4-7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lu et al. in the device of Wolk et al. to produce a semiconductor wafer with an embedded integrated circuit that has a decomposable layer that allows for secure bonding during the processing wafer while causing no damage (col. 2, lines 48-52).

Regarding claims **3** and **4**, Wolk et al. discloses a method for producing a semiconductor chip wherein the photothermal conversion layer, referred to as a light-to-heat conversion layer (LTHC), contains carbon black (col. 7, lines 27-33).

4. Claims **5**, **9** and **10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) and Lu et al. (US 7,226,812 B2) as applied to claim **1** above, and further in view of d'Aragona et al. (US 4,818,323).

Wolk et al. and Lu et al. fail to teach the limitation of laminating the semiconductor wafer in a vacuum.

However, d'Aragona et al. discloses a method for producing a semiconductor chip wherein laminating the wafer is performed in a vacuum (col. 2, lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of d'Aragona et al. with those of Wolk and Lu to laminate a wafer in a vacuum to insure the device will be free of voids.

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5. Claims 6, 7, 11-14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) and Lu et al. (US 7,226,812 B2) as applied to claims 1-4 above, and further in view of Miyakawa et al. (US 7,201,969 B2).

Wolk et al. and Lu et al. fail to teach the limitations disclosed in claims 6, 7, 11-14, 18 and 19.

Regarding claims **6**, **11** and **12**, Miyakawa et al. discloses that a semiconductor wafer can be ground or thinned until it is less than 200  $\mu\text{m}$  and has been thinned to about 50  $\mu\text{m}$  in some known cases (col. 3, lines 39-51).

Regarding claims **7**, **13** and **14**, Miyakawa et al. discloses that the storage elastic modulus of the base film, which is made of an adhesive layer (col. 6, lines 29-51), is between  $5 \times 10^8$  Pa to  $1 \times 10^{10}$  Pa (col. 7, lines 14-17).

Regarding claim **18**, Lu et al. discloses the use of a die bonding tape, referred to as protective tape, that is affixed to the semiconductor wafer before dicing (col. 6, lines 4-7) the ground wafer that Miyakawa et al. teaches that the wafer can be ground or thinned until it is about 50  $\mu\text{m}$  (col. 3, lines 39-51).

Regarding claim **19**, Lu et al. discloses the use of a die bonding tape, referred to as protective tape, that is affixed to the semiconductor wafer before dicing (col. 6, lines 4-7) the ground wafer that Miyakawa et al. teaches can be ground or thinned until it is about 50  $\mu\text{m}$  (col. 3, lines 39-51) and the storage modulus of the adhesive layer (col. 6, lines 29-51), is between  $5 \times 10^8$  Pa to  $1 \times 10^{10}$  Pa (col. 7, lines 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Miyakawa et al. in the method disclosed in Wolk et al. and Lu et al. to produce a semiconductor chip with a thickness of 50  $\mu\text{m}$  or less in order to meet the high demand for thinner semiconductor chips to be used in layered form (col. 3, lines 39-41) and

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that has a storage modulus of  $5 \times 10^8$  Pa or more after curing in order to have the strength to endure loads imposed in the direction of peeling during grinding (col. 6, lines 11-14). And so that the wafer ground wafer has a dicing tape bonded to it so the wafer can be diced in an adhered and secure condition to prevent the chips from being damaged during dicing.

6. Claims **8** and **15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) and Lu et al. (US 7,226,812 B2) as applied to claims 1-4 above, and further in view of Oka (US 6,551,906 B2).

Wolk et al. and Lu et al. fail to teach all limitations disclosed in claims 8 and 15-17.

However, Oka discloses a method wherein the dicing of a semiconductor wafer is performed along scribe lines, also referred to as cutting grooves (col. 5, lines 35-44; col. 4, lines 13-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Oka with those of Wolk et al. and Lu et al. in the device of so that the wafer is precisely diced with the use of scribe lines.

7. Claim **20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) and Lu et al. (US 7,226,812 B2) of as applied to claim **1** above, in view Oka (US 6,551,906 B2) and further in view of Miyakawa et al. (US 7,201,969 B2).

Wolk et al. and Lu et al. fail to teach all limitations disclosed in claim 20.

Oka discloses the use of a die bonding tape, referred to as a protective tape, that is affixed to the semiconductor wafer before dicing the ground wafer (col. 1, lines 46-59) and a method wherein the dicing of a semiconductor wafer is performed along scribe lines, also referred to as cutting grooves (col. 5, lines 35-44; col. 4, lines 13-20).

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However, Oka does not teach that the wafer can be ground to 50  $\mu\text{m}$  or less.

Miyakawa et al. does in fact teach that the wafer can be ground or thinned until it is about 50  $\mu\text{m}$  (col. 3, lines 39-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Miyakawa et al. and Oka with those of in the device of Wolk and Lu so that the wafer that has been ground, to a thickness of 50  $\mu\text{m}$  or less, is diced in an adhered and secure condition to prevent the chips from being damaged and so that the wafer is easily diced because of the scribing.

### ***Response to Arguments***

Applicant's arguments, see ***Remarks***, filed 11/30/07, with respect to the rejection(s) of claim(s) 1-20 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Lu et al. (US 7,226,812 B2).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENISHA V. FORD whose telephone number is (571)270-3328. The examiner can normally be reached on Monday-Thursday 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVF

/Michael S. Lebentritt/  
Supervisory Patent Examiner, Art Unit 2812